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(54) METHOD AND APPARATUS FOR ALLOCATING A COMMUNICATION RESOURCE IN A BROADBAND COMMUNICATION SYSTEM

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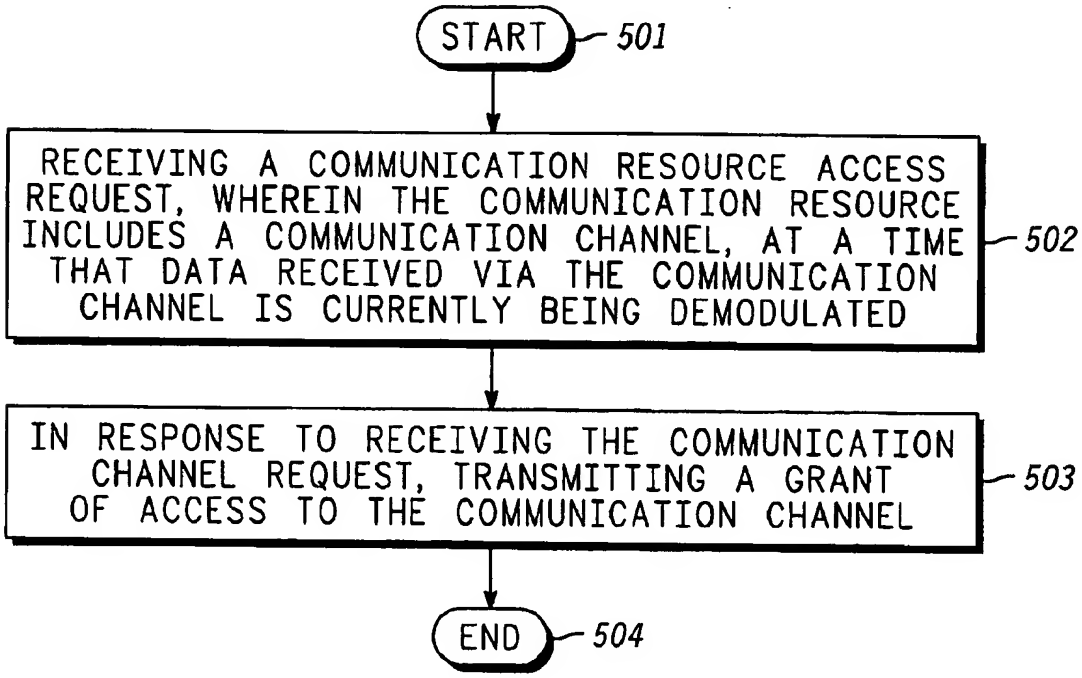
(57) ABSTRACT

A communication resource that includes a communication channel is allocated in response to a received communication resource access request, wherein the access request is received while a message received via the communication channel is being demodulated. In response to receiving the request, a grant of access to the communication channel is generated and transmitted, which grant authorizes the source of the access request to use the communication channel.



500

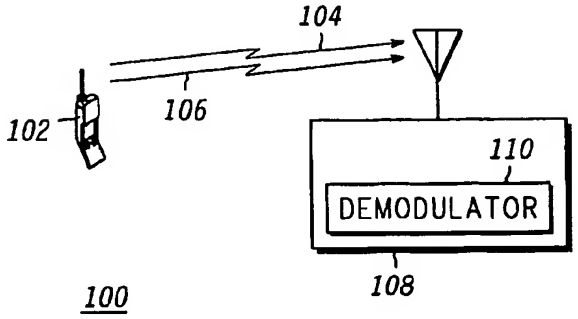
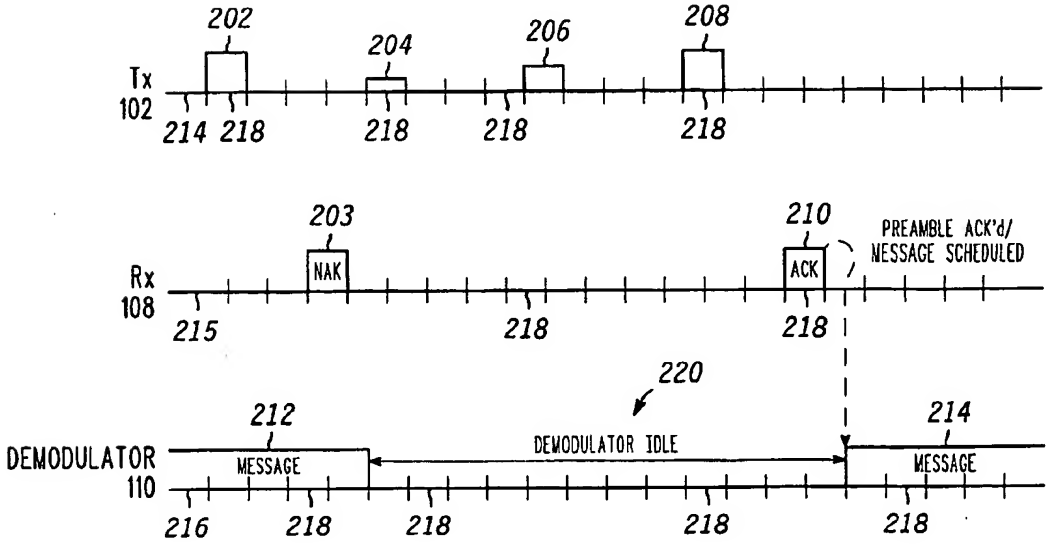


FIG. 1
-PRIOR ART-

200

FIG. 2
-PRIOR ART-



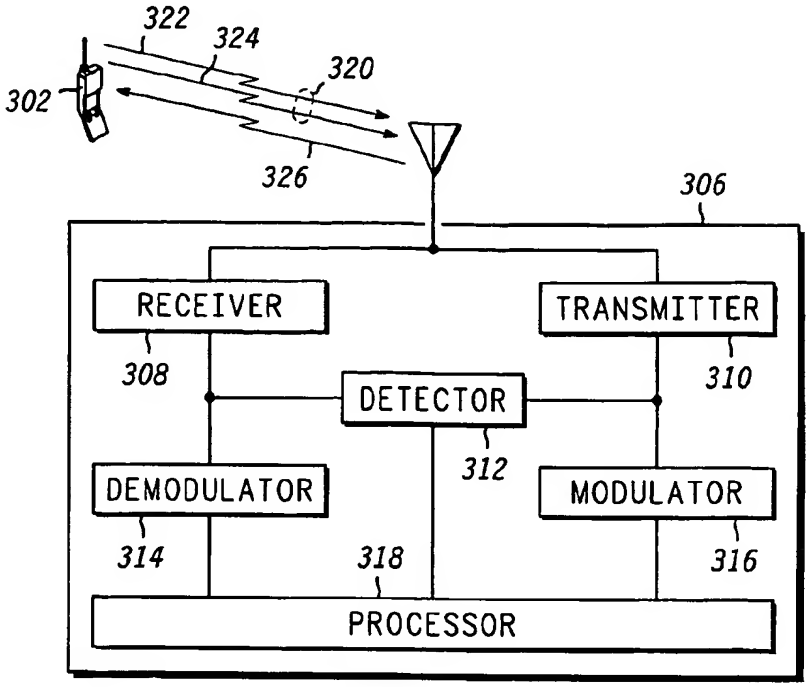
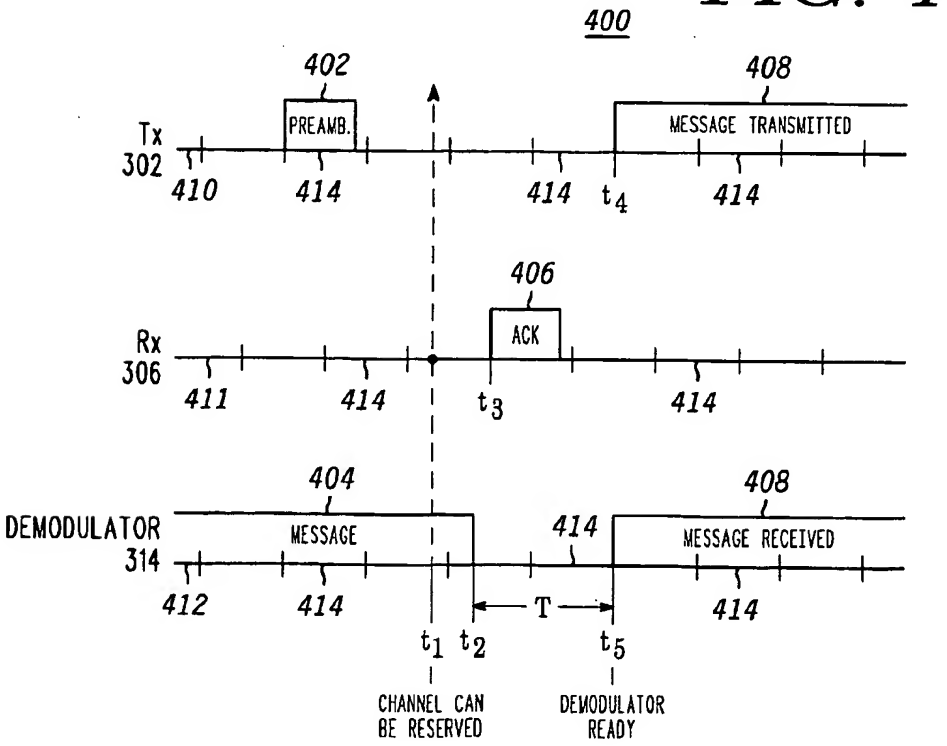


FIG. 3

300

FIG. 4



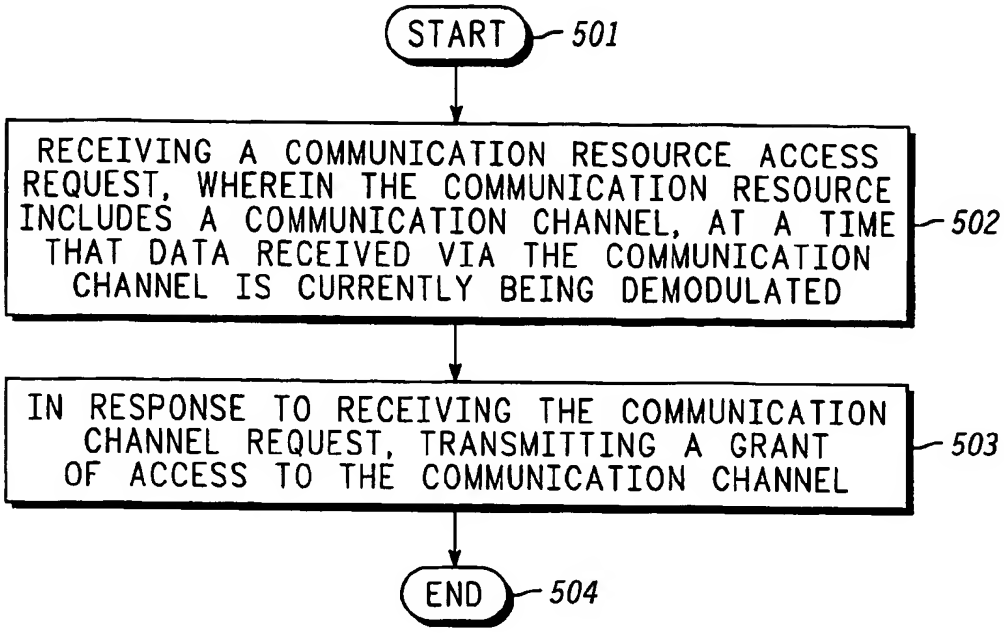

START
501
RECEIVING A COMMUNICATION RESOURCE ACCESS REQUEST, WHEREIN THE COMMUNICATION RESOURCE INCLUDES A COMMUNICATION CHANNEL, AT A TIME THAT DATA RECEIVED VIA THE COMMUNICATION CHANNEL IS CURRENTLY BEING DEMODULATED
502
IN RESPONSE TO RECEIVING THE COMMUNICATION CHANNEL REQUEST, TRANSMITTING A GRANT OF ACCESS TO THE COMMUNICATION CHANNEL
503
END
504

FIG. 5 500

METHOD AND APPARATUS FOR ALLOCATING A COMMUNICATION RESOURCE IN A BROADBAND COMMUNICATION SYSTEM

FIELD OF THE INVENTION

[0001] The present invention relates generally to cellular communication systems, and, in particular, to allocation of a communication resource in a broadband communication system.

BACKGROUND OF THE INVENTION

[0002] Wireless communication systems are well known and consist of many types, including land mobile radio, cellular radiotelephone, and personal communication systems. With each communication system, data is transmitted between a transmitting communication device and a receiving communication device via a communication resource that includes a communication channel that operates over a physical resource, typically a frequency bandwidth. Bandwidth is limited and equipment is expensive, and therefore many schemes have been developed for multiplexing many different users over the same frequency bandwidth.

[0003] One such communication system currently being developed is the next generation Code Division Multiple Access (CDMA) cellular communication system, commonly referred to as Wideband Code Division Multiple Access (WCDMA). In a WCDMA communication system, all mobile station and base station transmissions occur simultaneously within the same frequency band. Therefore, a received signal at a base station or a mobile station comprises a multiplicity of frequency and time overlapping coded signals from mobile stations or base stations, respectively. Each of the coded signals included in the received signal is transmitted simultaneously at the same radio frequency and is distinguishable only by the coded signal's specific orthogonal code (i.e., a communication channel).

[0004] A typical WCDMA communication system **100** of the prior art is shown in **FIG. 1**. Under current WCDMA Random Access Channel (RACH) standards, that is, European Telecommunications Standards Institute Technical Specifications (ETSI TS) 3GPP specifications TS25.215 and TS25.321, a mobile station (MS) **102** requests a first communication channel, that is, a reverse link traffic channel, **104** by transmitting a series of preambles via a second communication channel, that is, a reverse link control channel, **106** to a wireless infrastructure that includes a base station **108**. MS **102** adjusts the power level of each preamble of the series of preambles so that each preamble is transmitted at a different power level than the other preambles in the series of preambles. In turn, base station **108** grants MS **102** access to communication channel **104** by acknowledging a preamble that is received at an appropriate power level. Upon receiving an acknowledgment ('ACK') of a preamble from base station **108**, MS **102** transmits a message to the base station in communication channel **104**. In turn, so long as MS **102** fails to receive an acknowledgment of a preamble, MS **102** continues to transmit preambles to base station **108**.

[0005] By MS **102** varying the power levels of the preambles, and base station **108** acknowledging only an appropriately power-adjusted preamble, MS **102** and base station **108** are able to determine an appropriate power level for their communications. Thus the preambles serve both a power control function and an access request function. However, base station **108** will not acknowledge a preamble so long as a demodulator **110** in the base station is engaged in demodulation of a signal received via communication channel **104**. Instead, when base station **108** receives an appropriately power-adjusted access request and no communication channel is available, the base station transmits a NAK to MS **102**. In response to receiving the NAK, MS **302** backs off for a random period of time and then repeats the process of transmitting a series of successively incremented communication resource access requests.

[0006] For example, **FIG. 2** is a timing diagram **200** of an exemplary process of allocating a communication resource of the prior art. **FIG. 2** includes multiple time lines **214-216** that respectively correspond to MS **102**, base station **108**, and demodulator **110** and that are each subdivided into multiple time units **218**. Each time unit has a time duration of 1.33 milliseconds (ms), which is a typical length of an access slot, or preamble transmission, in a CDMA communication system.

[0007] As depicted in **FIG. 2**, MS **102** transmits a first preamble **202** at a time when demodulator **110** is demodulating a first message **212**. If preamble **202** is at an appropriate power level but demodulator **110** is engaged when base station **108** receives the preamble, the base station does not acknowledge the preamble (assuming that preamble **202** is at an appropriate power level) and instead transmits a NAK **203** to MS **102**. In response to receiving the NAK, MS **102** backs off for a random period of time and then repeats the process of transmitting a series of successively incremented preambles **204**, **206**, **208**. By the time base station **108** receives a second appropriately power-adjusted level preamble **208**, demodulator **110** has finished demodulating message **212**. Since demodulator **110** is now available to demodulate a new message, base station **108** transmits an ACK **210** back to MS **102**. Upon receiving ACK **210**, MS **102** transmits message **214** to base station **108**, which conveys the message to demodulator **110** for demodulation.

[0008] Since base station **108** does not acknowledge an appropriately power-adjusted preamble until demodulator **110** is available to demodulate a new message, the demodulator may be idle for a period of time **220** corresponding to awaiting receipt by the base station of a new, appropriately power-adjusted preamble **208**, acknowledgment by the base station of the new preamble, transmission of a message by the MS in response to receiving the acknowledgment, and receipt of the message by the base station. Such idle time is wasted time that reduces a throughput of communication channel **104** and a user capacity of system **100**. Furthermore, the repeated preamble transmissions consume a capacity of control channel **106**.

[0009] Therefore, a need exists for a method and an apparatus for communication resource allocation that reduces the idle time of a demodulator and that increases the throughput of a communication channel and the capacity of a broadband communication system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] **FIG. 1** is a block diagram of a communication system of the prior art.

[0011] **FIG. 2** is a timing diagram of an exemplary process of allocating a communication resource of the prior art.

[0012] FIG. 3 is a block diagram of a communication system in accordance with an embodiment of the present invention.

[0013] FIG. 4 is a timing diagram of an exemplary process of allocating a communication resource in accordance with an embodiment of the present invention.

[0014] FIG. 5 is a logic flow diagram of a method for allocating a communication resource in a broadband communication system in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] To address the need for a method and an apparatus for channel reservation that reduces the idle time of a demodulator and that increases the throughput of a communication channel and the capacity of a broadband communication system, a communication resource that includes a communication channel is allocated in response to a received communication resource access request, wherein the access request is received while a message received via the communication channel is being demodulated. In response to receiving the request, a grant of access to the communication channel is generated and transmitted, which grant authorizes the source of the access request to use the communication channel.

[0016] Generally, one embodiment of the present invention encompasses a method for allocating a communication resource in a broadband communication system, wherein the communication resource comprises a communication channel. The method includes steps of receiving a communication resource access request at a time that data received via the communication channel is currently being demodulated, and, in response to receiving the access request, transmitting a grant of access to the communication channel.

[0017] Another embodiment of the present invention encompasses an apparatus for allocating a communication resource in a broadband communication system, wherein the communication resource comprises a communication channel. The apparatus includes an access request detector that detects a receipt of a communication resource access request and a demodulator coupled to the access request detector is capable of demodulating messages received via the communication channel. The apparatus further includes a means for generating a grant of access to the communication channel and the demodulator in response to reception of the communication resource access request, wherein the communication resource access request is received at a time that the demodulator is engaged in a demodulation of a received message.

[0018] Still another embodiment of the present invention encompasses a communication device that is capable of operating in a broadband communication system. The communication device includes a receiver for receiving an communication resource access request and an access request detector coupled to the receiver that detects a receipt of the communication resource access request. The communication device further includes a demodulator coupled to the access request detector is capable of demodulating messages received via a communication channel and a means for generating a grant of access to the demodulator in response to reception of the communication resource access request, wherein the communication resource access request is received at a time that the demodulator is engaged in a demodulation of an already received message. The communication device further includes a modulator for modulating the access grant onto a radio frequency signal to produce a modulated access grant and a transmitter for transmitting the modulated access grant.

[0019] The present invention may be more fully described with reference to FIGS. 3-5. FIG. 3 is a block diagram of a communication system 300 in accordance with an embodiment of the present invention. Communication system 300 includes at least one mobile station (MS) 302 and a base station 306 that provides communications services to the MS. MS 302 and base station 306 are each capable of operating as a transmitting communication device or a receiving communication device in system 300. Base station 306 includes a receiver 308, a transmitter 310, an access request detector 312, preferably a preamble detection application specific integrated circuit (ASIC), coupled to the receiver, a demodulator 314 coupled to the receiver and the detector, a modulator 316 coupled to the transmitter, and a processor 318 coupled to each of the demodulator, the modulator, and the access request detector. Demodulator 314 demodulates a signal received by base station 306 based on a modulation scheme, such as a quadrature amplitude modulation (QAM) scheme, binary phase shift keying (BPSK) modulation scheme, or a quadrature phase shift keying (QPSK) modulation scheme, to produce a demodulated signal. Modulator 316 performs an inverse function to the function performed by demodulator 314, modulating a data stream received from processor 318 based on the modulation scheme to produce a modulated signal. In other embodiments of the present invention, processor 318 may include one of more of access request detector 312, demodulator 314, and modulator 316.

[0020] Communication system 300 preferably comprises a spread spectrum communication system, such as a wideband code division multiple access (WCDMA). A radio frequency (RF) communication resource 320 comprises a frequency bandwidth that includes multiple communication channels 322, 324 (two shown). Each communication channel of the multiple communication channels 322, 324 is covered by an orthogonal code sequence, preferably a Walsh Code, that is orthogonal to all other orthogonal code sequences that are transmitted in the frequency bandwidth. A transmitting communication device in system 300 transmits information by covering the information with the appropriate orthogonal code sequence and spreading the covered information with a pseudo-noise (PN) sequence to produce a spectrally spread signal. The spectrally spread signal is modulated pursuant to a modulation scheme, such as a quadrature amplitude modulation (QAM) scheme, binary phase shift keying (BPSK) modulation scheme, or a quadrature phase shift keying (QPSK) modulation scheme, to produce a modulated signal that is transmitted to a receiving communication device. In turn, the receiving communication device receives the modulated signal and demodulates the signal based on the modulation scheme applied by the transmitting communication device to produce a demodulated signal. The demodulated signal is despread with the PN sequence used to spread

the transmitted signal and uncovered by the channel assigned orthogonal code sequence in order to recover the transmitted information.

[0021] When MS **302** desires to access a communication channel **322**, preferably a reverse link traffic channel, of communication resource **320**, the MS transmits a series of communication resource access requests, preferably preambles, to base station **306** via a communication channel **324**, preferably a reverse link control channel, of the communication resource. The transmission of preambles to a base station in order to reserve a resource is described by current ETSI TS 3GPP specification TS25.213, which specification is hereby incorporated herein. MS **302** adjusts (typically increments) a power level of each access request of the series of access requests until receiving an 'ACK' (acknowledgment) or a 'NAK' back from base station **306**. Typically, each access request of the series of access requests is separated from an immediately preceding access request by a minimum of three or four access slots time units, wherein each access slot time unit has a time duration of 1.33 milliseconds (ms), which is a typical length of a preamble in a CDMA communication system.

[0022] When the access request is of an appropriate power level, base station **306** acknowledges the access request by transmitting an acknowledgment to MS **302**. Preferably, the acknowledgment is transmitted via a forward link control channel **326**; however, those who are of ordinary skill in the art realize that numerous methods of transmitting the acknowledgment exist. When MS **302** receives the acknowledgment, MS **302** understands that the most recently transmitted access request was at an appropriate power level for a transmission of a message. The acknowledgment also functions as an access grant by base station **306** in that MS **302** further understands, upon receiving the acknowledgment, that the MS is authorized to use, that is, is granted access to, communication channel **322** and, concomitantly, demodulator **314**.

[0023] By transmitting the series of access requests to base station **306** wherein the power level of each access request is different than the power levels of the other access request, and receiving an acknowledgment of an appropriately power-adjusted access request, MS **302** and base station **306** are able to determine an appropriate power level for a subsequent transmission of a message by the MS. Furthermore, by acknowledging an access request, base station **306** informs MS **302** that a traffic channel **322** and demodulator **314** are available for use by MS **102**.

[0024] In prior art communication system **100**, when demodulator **110** is currently engaged in demodulation of a message received via the communication channel and an appropriately power-adjusted preamble is received, the base station **108** transmits a NAK. That is, base station **108** will not acknowledge a preamble so long as demodulator **110** is engaged in demodulation of a received message, resulting in excessive demodulator idle time. In order to reduce the demodulator idle time and increase system capacity, base station **306** of communication system **300** can acknowledge the access request even while demodulator **314** is in the process of demodulating a received message.

[0025] When base station **306** receives an appropriately power-adjusted access request, the base station, preferably access request detector **312**, detects that an access request has been received. Access request detector **312** then communicates with processor **318** to determine whether the demodulator is available to demodulate a new message. If demodulator **314** is engaged in demodulation of a received message, such as user information data, then base station **306**, preferably processor **318**, determines an amount of time remaining until the demodulator is projected to be available. Alternatively, base station **306**, preferably processor **318** or alternatively access request detector **312** or demodulator **314**, may determine an amount of time remaining until demodulator **314** is projected to be available upon receipt of the message being demodulated or any time thereafter.

[0026] ETSI TS 3GPP specification TS25.216, which specification is hereby incorporated herein, provides that messages are transmitted in frames. The frames are of a known fixed length, or alternatively are of a variable length that is known to both the transmitting communication device and the receiving communication device. Based on when base station **306** begins receiving a message and further based on a known length of the message, base station **306**, preferably processor **318** or alternatively access request detector **312** or demodulator **314**, determines a time when demodulator **314** is projected to finish demodulating the received message and to be available to demodulate a new message.

[0027] In response to the receipt of the access request and based on the determined amount of time remaining until the demodulator is projected to be available, base station **306**, preferably processor **318** or alternatively access request detector **312**, generates an access grant and conveys the access grant to MS **302** via modulator **316** and transmitter **310**. The access grant preferably is an acknowledgment ('ACK') of the access request and is conveyed at a time that is designed to minimize the idle time of demodulator **314**. Preferably, the access grant is transmitted by base station **306** sometime during a time interval 'T' prior to the time that demodulator **314** is projected to be available. The time interval 'T' is determined based on a determined amount of time remaining until demodulator **314** becomes available and an amount of time required by MS **302** to receive an access grant, process the access grant, and transmit a message in response to the access grant. The amount of time required by MS **302** to receive an access grant, process the access grant, and transmit a message in response to the access grant may either be predetermined and programmed into base station **306** or may be determined by base station **306** through signaling with MS **302**. By transmitting the access grant at a time that is based on the projected availability of demodulator **314**, rather than waiting to consider an access request until the demodulator is actually available, base station **306** can coordinate a receipt of a new message from MS **302** with a projected freeing up of the demodulator, thereby minimizing the idle time of the demodulator.

[0028] For example, **FIG. 4** is a timing diagram **400** of an exemplary process of allocating a communication resource in accordance with an embodiment of the present invention. Timing diagram **400** assumes perfect channel conditions and zero propagation delay. **FIG. 4** is presented for the purpose of illustrating the principles of the present invention and is not intended to limit the invention in any way. **FIG. 4** includes multiple time lines **410-412** that respectively correspond to MS **302**, base station **306**, and demodulator **314** and that are each subdivided into multiple time units **414**.

Each time unit preferably has a time duration of 1.33 milliseconds (ms), which is an access slot, or preamble transmission, in a CDMA communication system.

[0029] As depicted in **FIG. 4**, MS **302** transmits an appropriately power adjusted communication resource access request **402**, preferably a preamble, at a time when demodulator **314** is demodulating a first message **404**. In response to the receipt of access request **402**, base station **306** determines a time t_2 when demodulator **314** will finish demodulating first message **404**. However, in other embodiments of the present invention, time t_2 and/or any one or more of time interval 'T' and times t_1, t_3, and t_5, as described below, may be determined at the time that base station **306** receives first message **404** or at any time thereafter.

[0030] Base station **306** determines time t_2 based on a known time when first message **404** was received by the base station and a known length of the first message. Based on time t_2, base station **306** determines a time t_5 when demodulator **314** will be available for demodulation of a second message **408**. Base station **306** further determines a time interval 'T'**420** corresponding to a projected time expiration between a conveyance, by base station **306** to MS **302**, of a grant of access to communication channel **322** and a receipt by the base station of a second message **408** from MS **302** in response to the access grant. The determination of time interval 'T'**420** is preferably based on an amount of time required by MS **302** to receive an access grant, preferably an ACK, **406**, process the ACK, and transmit second message **408** in response to receiving the ACK.

[0031] Based on the determined time t_5 and time interval 'T', base station **306** determines a time t_1 that corresponds to the earliest time that the base station can grant access to MS **302** to transmit a message in communication channel **322**. Base station **306** can then convey an access grant to MS **302** at the determined time t_1 or at any time thereafter in response to an appropriately power-adjusted access request, even if the access request is received when demodulator **314** is engaged in the demodulation of an already received message. For example, as depicted in **FIG. 4**, base station **306** transmits an access grant **406** at a time t_3 based on a receipt of access request **402**, even though demodulator **314** is engaged in the demodulation of message **404** when the access request is received. Optimally, base station **306** determines time t_3 such that MS **302** can receive the access grant, process the access grant, and transmit a second message **408** at a time t_4 that results in minimal demodulator **314** idle time (i.e., the time difference between time t_2 and time t_5).

[0032] By considering an access request **402** received prior to completion of demodulation of an earlier received message **404**, communication system **300** is able to reduce, relative to the prior art, idle time between modulation of the earlier received message and modulation of a subsequently received message. Base station **306** determines a time when demodulator **314** will be ready to demodulate a succeeding message based on a length of a received message **404**. Based on the determined ready time and a known access grant processing time of an MS **302**, base station **306** transmits an access grant to an MS **302** from which the base station has received an appropriate access request **402**. A timing of the transmission of access grant **406** is designed to minimize the idle time of demodulator **314** of base station **306**. By reducing the idle time, communication system **300** can operate at increased user capacity, and communication channel **322** can operate at increased throughput, relative to the prior art since a length of an idle, non-information bearing time period in system **300** is reduced.

[0033] **FIG. 5** is a logic flow diagram **500** of a method for allocating, in a broadband communication system, a communication resource that includes a communication channel in accordance with an embodiment of the present invention. The method begins (**501**) when a communication device receives (**502**) a communication resource access request, preferably a preamble, at a time that data received via the communication channel is currently being demodulated. In response to reception of the access request, the communication device transmits (**503**) a grant of access, preferably an acknowledgment, to the communication channel, and the logic flow ends (**504**). The access grant authorizes the source of the access request to use the communication channel. The transmission by the communication device of the access grant may occur either prior to completion of, upon completion of, or after completion of the demodulation of the data.

[0034] Preferably, the step of transmitting (**504**) a grant of access to the communication channel includes the following steps. The communication device determines a time that a demodulator will be available and determines a time that a grant of access to the communication channel can be transmitted based on the time that the demodulator will be available. The communication device then transmits an access grant based on the received request and on the determined time that the grant of access to the communication channel can be transmitted.

[0035] In other embodiments of the present invention, the step of transmitting (**504**) a grant of access to the communication channel may further include one or more of the following steps. The communication device may determine a time that the demodulator will finish demodulating the received message, then determining the time that the demodulator will be available based on the determined time that the demodulator will finish demodulating the received message. The communication device may also determine a time interval between the time that the demodulator will be available and a time that an access grant can be transmitted, then determining the time that an access grant can be transmitted based on the determined time interval.

[0036] In sum, a method and apparatus is provided for allocation of a communication resource that includes a communication channel in response to a received communication resource access request, wherein the access request is received while a message received via the communication channel is being demodulated. In response to receiving the request, a grant of access to the communication channel is generated and transmitted, which grant authorizes the source of the access request to use the communication channel.

[0037] While the present invention has been particularly shown and described with reference to particular embodiments thereof, it will be understood by those skilled in the art that various changes may be made and equivalents substituted for elements thereof without departing from the spirit and scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended

that the invention not be limited to the particular embodiments disclosed herein, but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. In a broadband communication system, a method for allocating a communication resource that comprises a communication channel, the method comprising steps of:

receiving a communication resource access request at a time that data received via the communication channel is currently being demodulated; and

in response to receiving the communication resource access request, transmitting a grant of access to the communication channel.

2. The method of claim 1, wherein the access grant is transmitted prior to completion of the demodulation of the data.

3. The method of claim 1, wherein the step of transmitting a grant of access to the communication channel comprises steps of:

determining a time that a demodulator will be available;

determining a time that a grant of access to the communication channel can be transmitted based on the time that the demodulator will be available; and

transmitting an access grant based on the received request and on the determined time that the grant of access to the communication channel can be transmitted.

4. The method of claim 3, wherein the step of transmitting a grant of access to the communication channel further comprises a step of determining a time that the demodulator will finish demodulating the received message.

5. The method of claim 3, wherein the step of transmitting a grant of access to the communication channel further comprises a step of determining a time interval between the time that the demodulator will be available and the time that an access grant can be transmitted.

6. The method of claim 1, wherein the communication resource access request is a preamble.

7. The method of claim 1, wherein the access grant is an acknowledgment.

8. An apparatus for allocating a communication resource in a broadband communication system, wherein the communication resource comprises a communication channel, the apparatus comprising:

an access request detector that detects a receipt of a communication resource access request;

a demodulator that is capable of demodulating messages received via the communication channel;

a means for generating a grant of access to the communication channel and the demodulator in response to reception of the communication resource access request; and

wherein the communication resource access request is received at a time that the demodulator is engaged in a demodulation of a received message.

9. The apparatus of claim 8, wherein the access grant is generated prior to completion of demodulation of the message.

10. The apparatus of claim 8, wherein the a means for generating a grant of access to the communication channel comprises:

a means for determining a time that the demodulator will be available;

a means for determining a time of transmission of a grant of access to the communication channel based on the determined time of demodulator availability; and

a means for generating an access grant based on the received communication resource access request and on the determined time of transmission of the access grant.

11. The apparatus of claim 10, wherein the means for generating a grant of access to the communication channel further comprises a means for determining a time that the demodulator will finish demodulating the received message.

12. The apparatus of claim 10, wherein the means for generating a grant of access to the communication channel further comprises a means for determining a time interval between the time that the demodulator will be available and the time that an access grant may be transmitted.

13. The apparatus of claim 8, wherein the access grant comprises an acknowledgment.

14. The apparatus of claim 8, wherein the communication resource access request comprises a preamble and wherein the access request detector comprises a preamble detector that detects a preamble in a received signal.

15. A communication device capable of operating in a broadband communication system, the communication device comprising:

a receiver for receiving an communication resource access request;

an access request detector coupled to the receiver that detects a receipt of the communication resource access request;

a demodulator coupled to the receiver that is capable of demodulating messages received via a communication channel;

a means for generating a grant of access to the demodulator in response to reception of the communication resource access request;

a modulator for modulating the access grant onto a radio frequency signal to produce a modulated access grant;

a transmitter for transmitting the modulated access grant; and

wherein the communication resource access request is received at a time that the demodulator is engaged in a demodulation of an already received message.

16. The communication device of claim 15, wherein the access grant is generated when the demodulator is engaged in a demodulation of an already received message.

17. The communication device of claim 15, wherein the a means for generating a grant of access to the communication channel comprises:

a means for determining a time that the demodulator will be available;

a means for determining a time of transmission of a grant of access to the communication channel based on the determined time of demodulator availability; and

a means for generating an access grant based on the received communication resource access request and on the determined time of transmission of the access grant.

18. The communication device of claim 17, wherein the means for generating a grant of access to the communication channel further comprises a means for determining a time that the demodulator will finish demodulating the received message.

19. The communication device of claim 17, wherein the means for generating a grant of access to the communication channel further comprises a means for determining a time interval between the time that the demodulator will be available and the time that an access grant may be transmitted.

20. The communication device of claim 15, wherein the communication resource access request comprises a preamble and wherein the access request detector comprises a preamble detector capable of detecting the preamble.

21. The communication device of claim 15, wherein the access grant comprises an acknowledgment.

* * * * *

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(54) **LOAD BASED CACHE CONTROL FOR SATELLITE BASED CPUS**

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(51) **Int. Cl.**[7] **G06F 12/00**

(52) **U.S. Cl.** **711/138**; 711/154; 364/152; 713/100; 455/12.1

(58) **Field of Search** 455/12.1; 364/140.01, 364/141, 148.01, 152; 711/118, 138, 152, 154, 163; 713/100; 714/825

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5,257,360 A * 10/1993 Schnizlein et al. 365/230.03
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6,081,868 A * 6/2000 Brooks 710/18

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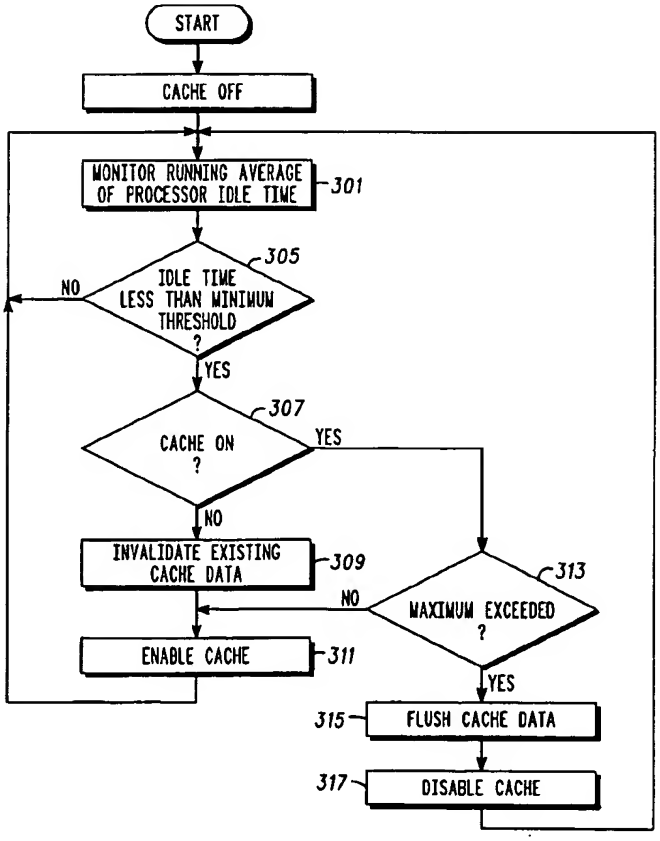
(57) **ABSTRACT**

The effect of Single Event Upsets (SEUs) occurring in cache memory (**103**) utilized in satellites is reduced. The idle time of a processor (**102**), utilizing cache memory (**103**), is monitored. If processor (**102**) idle time reaches a predetermined minimum (**205**), cache memory (**103**) is engage. When processor (**102**) idle time subsequently reaches a predetermined maximum threshold (**203**), cache memory (**103**) is disabled.

28 Claims, 2 Drawing Sheets



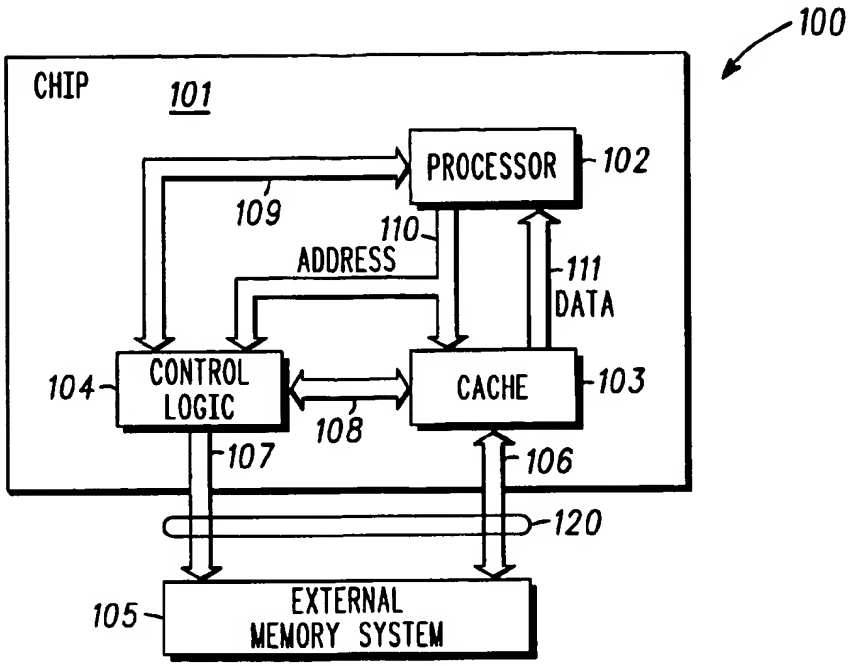

100
CHIP
101
PROCESSOR
102
109
110
ADDRESS
111
DATA
104
CONTROL LOGIC
CACHE
103
108
107
106
120
105
EXTERNAL MEMORY SYSTEM

FIG. 1

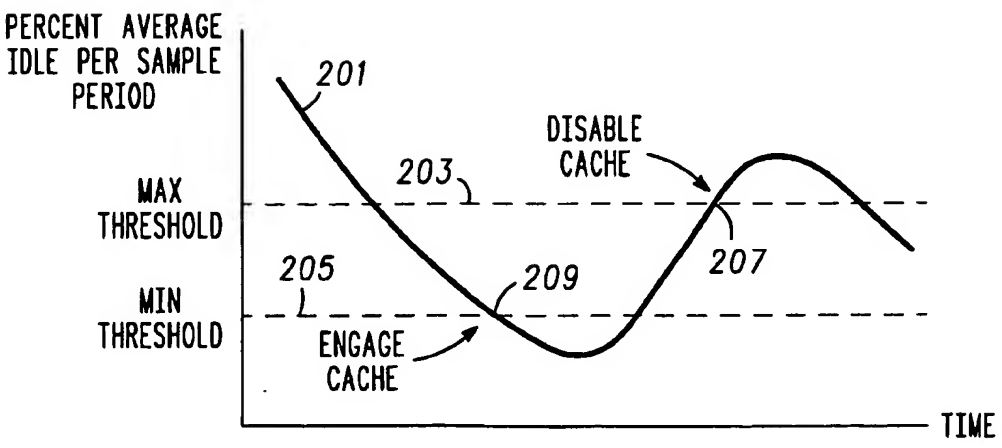

PERCENT AVERAGE IDLE PER SAMPLE PERIOD
201
DISABLE CACHE
203
MAX THRESHOLD
205
209
207
MIN THRESHOLD
ENGAGE CACHE
TIME

FIG. 2

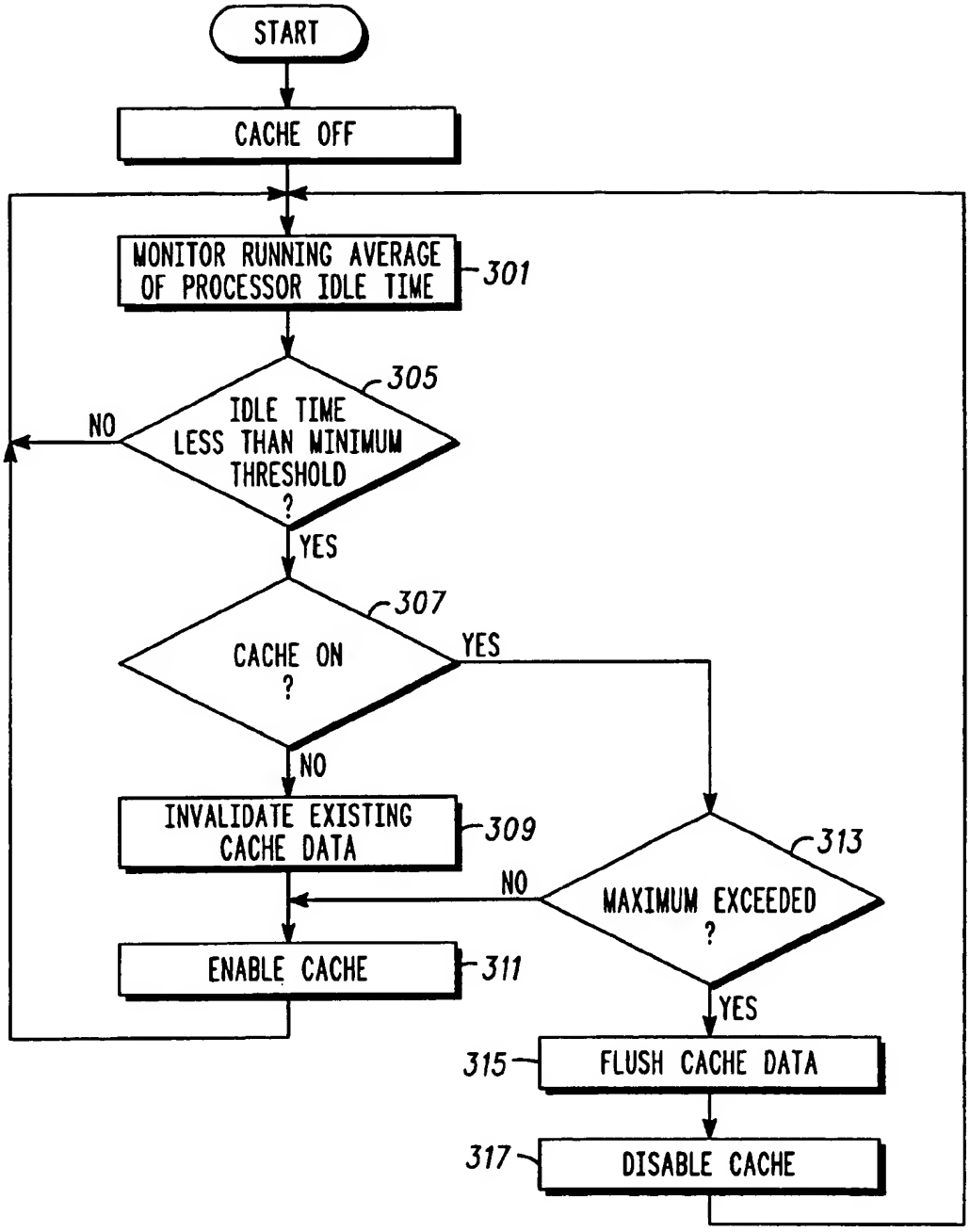

START
CACHE OFF
MONITOR RUNNING AVERAGE OF PROCESSOR IDLE TIME
301
305
IDLE TIME LESS THAN MINIMUM THRESHOLD ?
NO
YES
307
CACHE ON ?
YES
NO
INVALIDATE EXISTING CACHE DATA
309
313
MAXIMUM EXCEEDED ?
NO
ENABLE CACHE
311
YES
315
FLUSH CACHE DATA
317
DISABLE CACHE

FIG. 3

LOAD BASED CACHE CONTROL FOR SATELLITE BASED CPUS

FIELD OF THE INVENTION

This invention pertains to satellite communications, in general, and to the operation of satellite based central processing units having cache memory utilized in satellite communication systems, in particular.

BACKGROUND OF THE INVENTION

In order to increase the speed of processing within a microprocessor or central processing unit (CPU), designers implement cache memories within the microprocessor integrated circuit chip in order to compensate for the speed differential between main memory access time and processor logic. Processor logic is generally faster than main memory access time, with the result that processing speed is limited by the speed of main memory. A technique used to compensate for the mismatch in operating speeds is to employ an extremely fast small memory having an access time close to processor logic propagation delays between the CPU and main memory. This small, or cache, memory, is used to store segments of programs currently being executed in the CPU and/or temporary data frequently needed in immediate calculations. By making program instructions and data available at a rapid rate, it is possible to increase the performance of the processor.

A described in U.S. Pat. No. 5,918,247 issued to a common assignee, analysis of a large number of typical programs has shown that the references to memory during any given interval of time tend to be confined within a few localized areas in memory. This phenomenon is sometimes referred to as the property of "locality of reference." The reason for this property may be understood by considering that a typical computer program flows in a straight-line fashion with program loops and subroutine calls encountered frequently. When a program loop is executed, the CPU repeatedly refers to the set of instructions in memory that constitute the loop. Every time given subroutine is called, its set of instructions are fetched from memory. Thus, loops and subroutines tend to localize the reference to memory for fetching instructions.

If the active portions of the program and/or data are placed in a fast small memory, the average memory access time can be reduced, thus reducing the total execution time of the program. Such a fast small memory may be a cache memory or a buffer. Such a cache or buffer memory has an access time that is less than the access time of main memory, often by a factor of five to ten.

The fundamental idea of such a cache or buffer memory organization is that by keeping the most frequently accessed instructions and/or data in this fast cache or buffer memory, the average memory access time will approach the access time of the cache or buffer memory.

One problem with utilizing semiconductor components, such a microprocessors or CPUs, in a space environment is that the CPUs will be subjected to high energy rays or particles/ions. The geometries of newer integrated circuits are so small that passage of a high energy particle/ion or cosmic ray through a junction of a semiconductor device can cause an upset in the operation of the device. In such an environment, the presence of high energy rays or particles/ions causes random errors to occur in semiconductor devices. This problem is especially recurrent in semiconductor devices that have chips utilizing less than 3 micron geometry.

In memory systems, when a cosmic ray or high energy particle/ion passes through a sensitive junction of a storage element internal to a circuit, the result is an arbitrary change in the state of that storage element, i.e., a stored bit changes from a "zero" state to a "one" state, or vice versa. This phenomenon of a "one" change of state is called a "single event upset" (SEU). SEU is temporary in nature and disappears when the memory is reused for storing a new bit.

Due to severe irradiation effects occurring in the space environment, commercial processors can be vulnerable to the effects of SEU, which cause processor memory to become temporarily corrupted or changed. The more memory in a processor, the more susceptible it is to upset. Computer cache memory is a particularly SEU-sensitive component of a microprocessor or CPU used in space. Therefore, cache memories are often not used in satellite computers.

Not having a cache memory is a serious performance penalty to processors. Instruction and data cache memories can provide up to ten times performance improvement over similar non-cache memory operations. Therefore, non-cache memory operations can limit system capacity, performance and features offered by a given satellite.

Another way to avoid the effects of SEUs has been to use radiation hardened devices. Because the newest semiconductor devices having cache memory are not radiation hardened, satellite-based CPUs are often not the most recent commercial product.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood from a reading of the following detailed description of an embodiment of the invention taken, in conjunction with the drawings in which like reference designators used in the various figures are used to identify like elements, and in which:

FIG. **1** is a block diagram of a computer utilizing a cache memory to which the invention may be advantageously applied;

FIG. **2** is a graph illustrating enabling and disabling periods of a cache memory shown in the computer of FIG. **1**; and

FIG. **3** is a flow diagram illustrating operation of the computer of FIG. **1** in accordance with the principles of the invention.

DETAILED DESCRIPTION

In many satellite communication systems, processor loading is very peaky. While the satellite is over oceans, the satellite carries very little traffic. As the satellite moves over land masses, the load becomes very heavy and then tapers off again as the satellite moves over the North and South Poles. In addition, the region known as South Atlantic Anomaly (SAA) and the North and South Poles tend to be regions in which the highest amount of SEU activity occurs.

This invention utilizes the fact that processor performance can be measured in real time and that computer cache memory can be enabled and disabled in real time as well. For much of a satellite's orbit the satellite computers can, in accordance with the invention, have cache memories disabled, thereby making the computers more robust against the space environment, and only at those times where the load on the computers is increased are the cache memories engaged. During times in which the satellite is moving over the SAA and the Poles, the cache memories may be disengaged because of low computer activity. Thus, in accordance

with the invention, a dynamic cache memory control function is provided which has the benefit of making the satellite computer as robust as possible, while enabling maximum performance gains associated with the use of computer cache memory. A significant benefit of this approach is that commercial off-the-shelf processors, which are inexpensive and non-radiation-hardened, may be used in lieu of expensive and limited availability radiation-hardened processors. In addition, the use of newer and higher performance computing devices may be used to push the "technology envelope" in space applications. To effectively reduce the susceptibility of a computer to SEU in a space borne environment or any other alpha particle rich environment, the cache memory is dynamically controlled so as to enable the cache memory only when run time considerations require it. The cache memory is otherwise disabled. A run time load detection algorithm is used to dynamically engage or disengage cache memory based upon load considerations. The simple control algorithm trends the computer processor's idle time and, when the processor load increases such that idle time is below a threshold, cache memories are then engaged. Similarly, when the processor load relaxes, idle time increases to the point that a threshold is exceeded and the cache memories are disengaged. Hysterisis is provided near the separation in the set points so the cache memories are not thrashed in and out of operation.

Referring to FIG. **1**, a portion of a satellite communications system **100** including an integrated circuit chip **101** coupled by bus **120** to external memory **105**. Memory **105** may comprise any well-known memory device, such as RAM, ROM, disk storage devices or permanent storage devices. Within the following description, program instructions and data are often referred to separately, but both program instructions and data may be generally referred to as "data."

Chip **101** includes processor **102**, which may comprise a typical commercially available microprocessor or central processing unit. Coupled to processor **102** is a united cache memory **103**. Cache memory **103** may be a primary cache memory embedded within chip **101** or a secondary cache memory external to chip **101**. Further, cache memory **103** may be located anywhere along the path between processor **102** and external memory **105**, including being embedded within memory **105**. Cache memory **103** receives address information from processor **102** along bus **110** and transmits instructions and/or data information along bus **111** to processor **102**.

Chip **101** also includes control logic circuitry **104**. Control logic circuitry **104** communicates with processor **102** by bus **109**, receives the same address information sent via bus **110** from processor **102** to cache memory **103**, is coupled to cache memory **103** by bus **108** and is coupled to memory **105** by bus **107**, which may be part of bus **120**. Control logic circuitry **104**, like cache memory **103**, may be located external to chip **101**.

Processor **102** issues requests for data by issuing an address along bus **110** that is received by cache memory **103**. Cache memory **103** determines whether or not the requested data resides within cache memory **103**, and returns the requested data along bus **111** to processor **102** should cache memory **103** contain the requested data.

If the requested data does not reside within cache memory, **103**, a request for that data will be passed on to memory **105** along bus **120** in addition to a "fetch" being issued for the line containing the requested data. These requested will be sent to memory **105**, which will return the requested word and associated line of data to buffer **103** and processor **102**.

The basic operation of such a cache memory **103** is as follows: when processor **102** needs to access an instruction or data, cache memory **103** is examined. If the instruction or data word is found in cache memory **103**, it is read by processor **102**. If the word addressed by processor **102** is not found in cache memory **103**, memory **105** is accessed to read the data word. A block of words containing the one just accessed is then transferred from memory **105** to cache memory **103**. In this manner, some data is transferred to cache memory **103** so that future references to memory find the required words in cache memory **103**.

The average memory access time of the computer system is improved considerably by the use of cache memory **103**. The performance of cache memory **103** is frequently measured in terms of a quantity called a "hit ratio." When the CPU or processor **102** refers to memory and finds the word in cache memory **103**, it is said to produce a "hit." If the word is not found in cache memory **103**, it counts as a "miss." If the hit ratio is high enough so that most of the time processor **102** accesses cache memory **103** instead of memory **105**, the average access time is closer to the access time of cache memory **103**. For example, a computer with a cache memory access time of 100 nanoseconds, a main memory access time of 1,000 nanoseconds, and a hit ratio of 0.9 produces an average access time of 200 nanoseconds. This is a considerable improvement over a similar computer with a cache memory whose access time is 1,000 nanoseconds.

Processor **102** is operated by programs stored in memory **105**. The program function includes an idle time monitoring function or idle time monitor, which maintains a running average of idle time of processor **102**. As processor **102** idle time fluctuates, it will go above a maximum threshold and below a minimum threshold.

In FIG. **2**, a plot of processor percentage idle time is shown as curve **201**. As the percentage average idle time per sample period decreases, eventually a predetermined minimum threshold **205** is traversed at point **209**, at which time cache memory **103** is enabled. Cache memory **103** will remain enabled until the percentage average idle time per sample period reaches a predetermined maximum threshold **203** as indicated at point **207**, whereupon cache memory **103** is disabled. Cache memory **103** will remain disabled until the percentage average idle time again crosses minimum threshold **205**. The monitoring of processor activity or the average idle time per sample period is, in the illustrative embodiment, performed by processor **102** utilizing a program stored in memory **105**. The idle time monitor, as it may be called, operates such that when the percentage average idle time becomes less than a minimum threshold **205**, thereby indicating a heavy load period, cache memory **103** is enabled. When the percentage average idle time is determined to be above a subsequent maximum threshold **203**, cache memory **103** is disabled during the corresponding low usage period.

The present invention provides for separate low and high thresholds **205**, **203**, respectively, which provide hysterisis. The delta or change between the minimum idle time threshold **205** and the maximum idle time threshold **203** may be referred as to as the "hysterisis valley," and is configured to be large enough to prevent small changes in idle time, which would result in a change in the enabled or disabled state of cache memory **103**. Rapid enabling and disabling of cache memory **103** due to small changes in idle time is referred to as "thrashing." To achieve stability of cache memory **103** over time, it is necessary to prevent thrashing. The selection of threshold **205** and **203** is made to delay enabling and

disabling cache memory **103** until enough time has elapsed to necessitate a change in the status of cache memory **103**, thereby avoiding thrashing.

Turning to FIG. **3**, processor **102** continuously monitors its activity by monitoring the running average of processor idle time at step **301**. The idle time monitor function provided by processor **102** and the program in memory **105** is utilized to determine when processor **102** idle time has decreased to less than the minimum threshold **205** at step **305**. If the idle time is not less than a predetermined minimum, processor **102** continues to monitor the average running time as indicated at step **301**. When minimum threshold **205** is exceeded as indicated at step **305**, a determination is made as to whether cache memory **103** is enabled at step **307**. If cache memory **103** is not enabled at this time, processor **102** invalidates the existing data in cache memory **103** at step **309**, and processor **102** enables cache memory **103** at step **311**. After cache memory **103** is thus enabled, the process will return to step **301** to continue to monitor average processor idle time. If, at step **305**, it is determined that the idle time is less than predetermined level **205** and cache memory **103** is enabled as indicated at step **301**, a determination is made to determine if the idle time has reached maximum threshold **203** at step **313**. If maximum threshold **203** is not exceeded, cache memory **103** is enabled as indicated at step **311**. If maximum threshold **203** is reached as indicated at step **313**, processor **102** flushes cache memory **103** at step **315**. Cache memory **103** is then disabled at step **317**. The process returns to monitoring step **301**.

As will be appreciated by those skilled in the art, the idle time monitor is a function which is readily implemented in software, as is the setting of software thresholds for idle time. It is specifically contemplated that he present invention will encompass additional implementations, including hardware, software or a combination of hardware and software. It will be further appreciated that cache memory **103** may be enabled or disabled based upon the position of the satellite. For example, cache memory **103** may be disabled when a satellite is passing over polar regions or the SAA.

As will be understood by those skilled in the art, the invention has been described in conjunction with a specific embodiment and that various changes and modifications may be made to the embodiment without departing either from the spirit or scope of the invention. It is not intended that the invention be limited to the specific embodiment shown and described, but that the invention be limited in scope only by the claims appended hereto.

What is claimed is:

1. A method of operating a computer to minimize single event upsets, such computer comprising a processor, a memory containing programs for operations said processor and a cache memory coupled to said processor, said method comprising:

monitoring idle time of said processor;

identifying a predetermined idle time threshold; and

controlling said cache memory when said idle time reaches said predetermined idle time threshold.

2. A method in accordance with claim **1**, wherein:

said controlling step comprises enabling said cache memory.

3. A method in accordance with claim **2**, comprising:

identifying a second predetermined idle time threshold; and

disabling said cache memory when said idle time reaches said second predetermined idle time threshold.

4. A method in accordance with claim **3**, comprising:

selecting said predetermined idle time threshold and said second predetermined idle time threshold so as to provide hysterisis.

5. A method in accordance with claim **1**, wherein:

said controlling step comprises disabling said cache memory.

6. A method in accordance with claim **1**, comprising:

operating said computer in an extraterrestrial vehicle.

7. A method in accordance with claim **1**, comprising:

operating said computer in a satellite vehicle.

8. A method in accordance with claim **7**, comprising:

using said computer to control satellite communication functions.

9. A method in accordance with claim **1**, wherein:

said processor and said cache memory are on an integrated circuit chip.

10. A satellite vehicle comprising:

a processor;

cache memory coupled to said processor; and

an idle time monitor monitoring an average idle time of said processor, said idle time monitor controlling said cache memory when said processor average idle time reaches a predetermined idle time threshold.

11. A satellite vehicle in accordance with claim **10**, wherein:

said idle time monitor enables said cache memory when said processor average idle time reaches said predetermined idle time threshold.

12. A satellite vehicle in accordance with claim **10**, wherein:

said idle time monitor disables said cache memory when processor idle time reaches said predetermined idle time threshold.

13. A satellite vehicle in accordance with claim **12**, wherein:

said idle time monitor enables said cache memory when said processor average idle time reaches a second predetermined idle time threshold.

14. A satellite vehicle in accordance with claim **10**, comprising:

a memory coupled to said processor; and

said idle time monitor comprises a program resident in said memory.

15. A satellite vehicle in accordance with claim **10**, wherein:

said processor and said cache memory are both on a single integrated circuit chip.

16. A computer comprising:

a processor;

a cache memory coupled to said processor; and

an idle time monitor monitoring an average idle time of said processor and controlling said cache memory when said processor average idle time reaches a predetermined threshold.

17. A computer in accordance with claim **16**, wherein:

said controlling comprises enabling said cache memory.

18. A computer in accordance with claim **16**, wherein:

said controlling comprises disabling said cache memory.

19. A computer in accordance with claim **16**, wherein:

said cache memory is enabled when said processor average idle time reaches said predetermined threshold and is disabled when said processor average idle time reaches a second predetermined threshold.

20. A computer in accordance with claim 16, wherein:

said processor and said cache memory are both on a single integrated circuit chip.

21. A method of operating a computer comprising a processor and a cache memory, said computer being in a satellite vehicle in earth orbit, said method comprising the steps of:

determining periods of time occurring during said earth orbit of said satellite vehicle during which processor idle time is high; and

disabling said cache memory during said periods.

22. A method in accordance with claim 21, comprising:

enabling said cache memory when said processor idle time is below a predetermined threshold.

23. A method in accordance with claim 21, wherein:

said satellite vehicle is a communication satellite; and

said periods of idle time occur when said satellite vehicle is in predetermined positions relative to the earth.

24. A method in accordance with claim 23, wherein:

said predetermined positions include when said satellite vehicle is traversing polar regions of the earth.

25. A method in accordance with claim 24, wherein:

said predetermined positions include satellite positions over a South Atlantic Anomaly.

26. A method in accordance with claim 25, comprising:

enabling said cache memory when said processor idle time is below a predetermined threshold.

27. A method in accordance with claim 23, wherein:

said predetermined positions include satellite positions over a South Atlantic Anomaly.

28. A method in accordance with claim 27, comprising:

enabling said cache memory when said processor idle time is below a predetermined threshold.

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